IN THE CLAIMS

1. (Currently Amended) A semiconductor memory device comprising:

a plurality of memory cells arranged in rows and columns;

a plurality of bit lines, disposed corresponding to the columns of the memory cells, each having the memory cells on a corresponding column coupled ~~connected~~; and

a plurality of bit line drive circuits disposed corresponding to the bit lines and supplying currents according to write data to a corresponding bit line, each bit line drive circuit including; a first drive circuit for supplying a first current to a corresponding bit line in accordance with write data to an adjacent column when the adjacent column is selected; and a second drive circuit for supplying a second current to the corresponding bit line in accordance with the write data to the corresponding column when the corresponding column is selected.

2. (Original) The semiconductor memory device according to claim 1, wherein said first current is smaller than said second current.

3. (Original) The semiconductor memory device according to claim 1, wherein

when the adjacent column is selected, said first drive circuit causes said first current to flow in a direction opposite to a direction of a current flowing in said adjacent column.

4. (Original) The semiconductor memory device according to claim 1, further comprising:

a column selecting circuit for selecting a predetermined number of bit lines in parallel from said plurality of bit lines in accordance with an address signal, any adjacent bit lines in said predetermined number of bit lines sandwiching at least one bit line; and

a write circuit for transmitting data bits in parallel to said predetermined number of bit lines selected in parallel.

5. (Original) The semiconductor memory device according to claim 4, wherein

said column selecting circuit includes at least a circuit for simultaneously selecting two bit lines sandwiching one bit line, and

said first drive circuit includes:

a detector for detecting match of logic levels of write data to bit lines adjacent on both sides in a row direction; and

a driver for supplying said first current in accordance with a column selection signal to the bit lines adjacent on said both sides and an output signal of said detector.

6. (Original) The semiconductor memory device according to claim 4, wherein

said first drive circuit stops supplying said first current when bit lines adjacent in a row direction are both selected and logic levels of write data to the adjacent bit lines on the both sides are different from each other.

7. (Original) The semiconductor memory device according to claim 4, wherein

said first drive circuit increases said first current when bit lines adjacent in a row direction on both sides are both selected and logic levels of write data to said the adjacent bit lines on the both sides are identical.

8. (Original) The semiconductor memory device according to claim 1, wherein each bit line drive circuit has right-side and left-side drive circuits, disposed on both sides of a corresponding bit line respectively, operating complementary to each other to cause currents to flow in the corresponding bit line in opposite directions.

9. (Original) A semiconductor memory device comprising:

a plurality of magnetic memory cells arranged in rows and columns;

a plurality of bit lines, disposed corresponding to the columns of said plurality of magnetic memory cells, each coupling ~~connecting~~ to the memory cells of a corresponding column;

a column selecting circuit for selecting a predetermined number of memory cell columns in parallel from the columns of said plurality of magnetic memory cell in accordance with an address signal, said any adjacent columns in said predetermined number of memory cell columns sandwiching at least one bit line; and

a plurality of bit line drive circuits disposed corresponding to the bit lines and supplying a current to a corresponding bit line in accordance with write data and a column selection signal from said column selecting circuit.

10. (Original) The semiconductor memory device according to claim 9, wherein each bit line drive circuit has right-side and left-side drive circuits disposed on both sides of a corresponding bit line respectively and operating complementary to each other to cause currents to the corresponding bit line in opposite directions.

11. (Original) The semiconductor memory device according to claim 9, wherein each bit line drive circuit includes a cancel circuit for supplying, when a bit line of an adjacent column is selected, a current to a corresponding bit line so as to cancel out an influence of a magnetic field induced by a current flowing in the adjacent column on a magnetic memory cell of the corresponding column.

12. (Currently Amended) A semiconductor memory device comprising:

a plurality of memory cells arranged in rows and columns;

a plurality of bit lines, disposed corresponding to the columns of the memory cells, each having the memory cells on a corresponding column coupled ~~connected~~; and

bit line drive circuitry for supplying current according to write data to a corresponding bit line coupling ~~connecting~~ to a memory cell having said write data written thereinto, said bit line drive circuitry including; a first drive circuit for supplying a first current to the corresponding bit line in accordance with write data to an adjacent column when the adjacent column is selected; and a second drive circuit for supplying a second current to the corresponding bit line in accordance with the write data to a corresponding column when the corresponding column is selected.

13. (Previously Presented) The semiconductor memory device according to claim 12, wherein said first current is smaller than said second current.

14. (Previously Presented) The semiconductor memory device according to claim 12, wherein

15. (Previously Presented) The semiconductor memory device according to claim 12, further comprising:

a column selecting circuit for selecting a predetermined number of bit lines in parallel from said plurality of bit lines in accordance with an address signal, any adjacent bit lines in said predetermined number of bit lines sandwiching at least one bit line; and

a write circuit for transmitting data bits in parallel to said predetermined number of bit lines selected in parallel.

16. (Previously Presented) The semiconductor memory device according to claim 15, wherein

said column selecting circuit includes at least a circuit for simultaneously selecting two bit lines sandwiching one bit line, and

said first drive circuit includes:

a detector for detecting match of logic levels of write data to bit lines adjacent on both sides in a row direction; and

a driver for supplying said first current in accordance with a column selection signal to the bit lines adjacent on said both sides and an output signal of said detector.

17. (Previously Presented) The semiconductor memory device according to claim 15, wherein

said first drive circuit stops supplying said first current when bit lines adjacent in a row direction are both selected and logic levels of write data to the adjacent bit lines on the both sides are different from each other.

18. (Previously Presented) The semiconductor memory device according to claim 15, wherein

said first drive circuit increases said first current when bit lines adjacent in a row direction on both sides are both selected and logic levels of write data to said the adjacent bit lines on the both sides are identical.